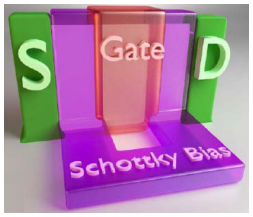
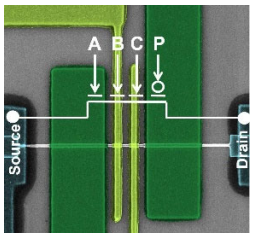
Diploma/Master Thesis

Title: **Electrical Transport in Steep-Slope Schottky Ge-FinFETs**
Institute: Institute of Solid State Electronics
Supervisor: Prof. Walter M. Weber
Languages: German, English

Description:





In the quest for energy efficient integrated circuits, considerable focus has been devoted on steep-slope and polarity-controllable transistors, targeting low supply voltages and a reduction of transistor count. Multi-gated silicon devices have shown the ability to operate at ultra-steep subthreshold slopes by combining impact ionization and positive feedback.[1] The use of germanium channels holds the promise for even higher efficiencies to be explored experimentally in this thesis. To facilitate the concept of multi-gate Ge FETs with precisely defined Schottky junctions, we have established a thermally induced exchange reaction in the Al-Ge material system.[2] This process enables the synthesis of metal-semiconductor-metal heterostructures based on Ge nanowires or nanosheets. Tuning the parameters of this heterostructure formation technique allows the fabrication of devices with ultra-short channel lengths beyond lithographic limitations and atomically sharp metal-semiconductor interfaces, enabling the exploration of novel electrical transport phenomena. The duration of the master thesis is 6 months with a payment according to the FWF scholarship (438,05 €/month).

(1) Journal of Applied Physics 121, 064504 (2017)
(2) Journal Electron Device Society, 452-456 (2015)

Scope of the work:

- Exploration of new device architectures (multi-gate devices)
- Advanced electrical characterization and distinction between the different transport operation regimes: thermionic emission, tunneling, impact ionization and positive feedback at ambient conditions and cryogenic temperatures

Who can apply:

The cross-disciplinary nature of the projects invites students with background in microelectronics, physics and material science.

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